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10/632,214	07/31/2003	Gerard Chauvel	TI-35427	1113

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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
06/23/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/632,214	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,8-11,13,15 and 18-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9 and 10* is/are rejected.

7)☒ Claim(s) *1,3,5,8,11,13,15 and 18-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3, 5, 8-11, 13, 15, and 18-22 are pending.

2. The office acknowledges the following papers:

Arguments, specification, and claims filed on 5/12/2009.

Allowable Subject Matter

3. Claims 1, 3, 5, 8, 11, 13, 15, and 18-22 would be allowable if rewritten or amended to overcome the claim objections, set forth in this Office action.

Claim objections

4. Claims 1, 8-9, 11, and 19-20 are objected for the following reasons:

5. Claim 1 recites "an arithmetic logic unit" at line 3 that should be changed to "an arithmetic logic unit (ALU)" for proper antecedent basis for "the ALU" at line 4.

6. Claim 1 recites "said instruction" at lines 7 and 9 that should be changed to "said test and skip instruction" for proper antecedent basis.

7. Claim 1 recites "the masked version" at lines 21-22 that should be changed to "[[the]] a masked version" for proper antecedent basis.

8. Claim 8 recites "the registers" at line 1 that should be changed to "the plurality of registers" for proper antecedent basis.

9. Claim 8 recites "the masked version" at line 7-8 that should be changed to "[[the]] a masked version" for proper antecedent basis.

10. Claim 9 recites "the outcome" at lines 8 and 13 that should be changed to "[[the]] an outcome" for proper antecedent basis.

11. Claim 9 recites "the second group of registers" at line 11 that should be changed to "[[the]] a second group of registers" for proper antecedent basis.

12. Claim 11 recites "the register value" at line 9 that should be changed to "[[the]] a register value" for proper antecedent basis.

13. Claim 11 recites "said at least one bit" at lines 15-16 and 18 that should be changed to "said at least one register reference control bit" for proper antecedent basis.

14. Claim 11 recites "the masked version" at line 20 that should be changed to "[[the]] a masked version" for proper antecedent basis.

15. Claim 19 recites "the processor" at line 9 that should be changed to "the [[processor]] programmable logic device" for proper antecedent basis.

16. Claim 19 recites "said control bit" at lines 11 and 17 that should be changed to "said register reference control bit" for proper antecedent basis.

17. Claim 19 recites "the masked version" at lines 14-15 that should be changed to "[[the]] a masked version" for proper antecedent basis.

18. Claim 20 recites "the system" at line 1 that should be changed to "the [[system]] programmable logic device" for proper antecedent basis.

New Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claim 9 is rejected under 35 U.S.C. §103(a) as being unpatentable over Terada et al. (U.S. 6,041,399), in view of Blaner et al. (U.S. 5,659,722), in view of Weaver et al. ("The SPARC Architecture Manual: Version 9").

21. As per claim 9:

Terada disclosed a method of executing an instruction defined by an opcode, an immediate value, and a register reference control bit contained within a source operand of the instruction that dictates one of at least two tests, the method comprising:

examining said register reference control bits to determine its state (Terada: Figure 4, column 5 lines 66-67 continued to column 6 lines 1-24)(The opcode of the instruction specifies how the instruction will execute, which equates to the register reference control bits.);

if said register reference control bits are in a first state, comparing the immediate value to the contents of a register in a first group of registers and skipping a subsequent instruction based on the outcome of the comparison (Terada: Figure 4, column 5 lines 66-67 continued to column 6 lines 1-24)(The compare instruction in figure 4 is done by comparing the data stored in the specified register to the immediate value. The register is a normal register within the register file and is not the status register. Thus having the same functionality.); or

Terada failed to teach if said register reference control bit is in a second state, masking the contents of a register in a second group of registers with the immediate

value, testing one or more bits in the masked version of the contents of the register, and skipping a subsequent instruction based on the outcome of the testing; and wherein said register reference control bit is outside said opcode.

However, Blaner disclosed if said register reference control bits are in a second state, masking the contents of a register in a second group of registers with the immediate value, testing one or more bits in the masked version of the contents of the register, and skipping a subsequent instruction based on the outcome of the testing (Blaner: Figures 3 and 7, column 4 lines 53-67 continued to column 5 lines 1-42 and column 6 lines 26-39 and column 8 lines 4-31)(The test and branch instruction's opcode states that the comparison is done between the status register and the immediate predicate value within the instruction, which is element 508 in figure 3. Figure 7 shows the process of executing this instruction. Element 330 is the status register that stores the current status bits that are checked by the branch instruction. Column 8 discusses the process of masking the immediate mask in the instruction with the status register values to determine test value. This test value is the basis of if the branch is taken or not.).

Processing elements produce condition signals during execution that indicate conditions relevant to the execution of an instruction. These signals can later be used by conditional branches to determine if certain conditions were met for a branch instruction (Blaner: Column 1 lines 20-29). This type of branch instruction that performs a mask of the status bits with an immediate value to determine if the branch is taken would also be useful in other processors, such as the processor of Terada. The

advantage of having conditional branches that branch on the status bits generated from prior instructions would have motivated one of ordinary skill in the art at the time of the invention to implement the test and branch instruction of Blaner into the processor of Terada. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add the test and branch instruction to Terada for the benefits of branching dependent on different status bits generated from previous instructions.

Terada and Blaner failed to teach a register reference control bit that specifies a first or second state and wherein said register reference control bit is outside said opcode.

However, Weaver disclosed a register reference control bit that specifies a first or second state and wherein said register reference control bit is outside said opcode (Weaver: Figure 33, pages 64, 138-139, and 146-150)(The SPARC manual shows branch instructions with a common opcode and a rcond code that specifies a specific type of branch instruction. The combination with Terada and Blaner allows for the two instructions to share an opcode and have control bits outside of the opcode to specify which operation will execute. An individual bit within the rcond code is the register reference control bit that allows for the selection of two operations given the other bits are the same value.).

The advantage of using control bits outside of an instruction opcode to specify execution is that is can be used to expand a processor's instruction set architecture for operations that have unused bits in their instruction encoding. One of ordinary skill in the art would have been motivated by this to allow for control bits outside of the

instruction opcode to specify different operations for the advantage of expanding a processor's instruction set architecture. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement control bits outside of the instruction opcode for the advantage of expanding a processor's instruction set architecture.

22. Claim 10 is rejected under 35 U.S.C. §103(a) as being unpatentable over Terada et al. (U.S. 6,041,399), in view of Blaner et al. (U.S. 5,659,722), in view of Weaver et al. ("The SPARC Architecture Manual: Version 9"), further in view of Chen et al. (U.S. 5,504,903)

23. As per claim 10:

Terada, Blaner, and Weaver disclosed the method of claim 9.

Terada, Blaner, and Weaver failed to teach wherein skipping the subsequent instruction comprises replacing the subsequent instruction with a no operation instruction.

However, Chen disclosed wherein skipping the subsequent instruction comprises replacing the subsequent instruction with a no operation instruction (Chen: Column 7 lines 59-67 continued to column 8 lines 1-3).

Both the bit test and skip if set/clear instructions are essentially a predicated compare instruction, which will only execute the next instruction if a condition is met. If the condition is met, then the next instruction is not allowed to complete and is essentially the same as a nop instruction. Thus, it would have been obvious to one of

ordinary skill in the art to use the process from Chen of substituting in a nop instruction instead of the instruction from Blaner or Terada that will simply not complete if the condition to not execute is met.

Response to Arguments

24. The arguments presented by Applicant in the response, received on 5/12/2008 are partially considered persuasive.

25. Applicant argues "The amended independent claims contain limitations that the "register reference control bit is contained within a source operand of the instruction". The Action suggested that these limitations would overcome all rejections" for claims 1, 9, 11, and 19.

This argument is found to be persuasive for the following reason. The examiner agrees that independent claims 1, 11, and 19 are now allowable due to the amendment of the examiner's suggestion. This limitation upon an updated search has not been found in the prior art.

In response to applicant's arguments for claim 9, the recitation "register reference control bit contained within a source operand of the instruction" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural

limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

26. Applicant argues "Amended claim 9 now limits the comparing or masking to a register in a first or second group of registers. This overcomes the rejections based on 35 USC 112, first paragraph" for claim 9.

This argument is found to be persuasive for the following reason. The amendment clears up the enablement problems with claim 9 and the rejections based on 35 USC 112 first and second paragraphs have been withdrawn.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Jacob Petranek
Examiner, Art Unit 2183